What is claimed is:

1. A storage device comprising:

plural groups of memory cells, wherein the memory cells comprise magnetoresistive elements,

wherein each group further includes a corresponding transistor, and the memory cells of each group includes a first set of parallel connected memory cells connected to a node of the transistor; and

a sensing device to detect a state of a memory cell in a selected one of the groups.

2. The storage device of claim 1, wherein each group further comprises a second set of parallel connected memory cells.

3. The storage device of claim 2, wherein the first set of memory cells comprises memory cells coupled in parallel between a first bias signal and a common node, and wherein the second set of memory cells comprises memory cells coupled in parallel between a second bias signal and the common node.

4. The storage device of claim 3, wherein the common node is connected to a gate of the transistor, and wherein a source of the transistor is coupled to the sensing circuit.

5. The storage device of claim 4, wherein a drain of the transistor is coupled to a supply voltage.

6. The storage device of claim 3, further comprising a bit line, wherein the transistor forms a pass gate, a first source/drain node of the transistor connected to the common node, a second source/drain node of the transistor connected to the bit line, and a gate of the transistor connected to a select signal.

7. The storage device of claim 1, further comprising a bit line connected to the groups of memory cells, the sensing device coupled to the bit line.

8. The storage device of claim 7, wherein the transistor of one of the groups of memory cells connected to the bit line is activated while the transistors of the remaining groups of memory cells connected to the bit line are deactivated.

9. The storage device of claim 7, further comprising a second bit line coupled to further groups of memory cells, the storage device further comprising a second sensing circuit coupled to the second bit line.

10. The storage device of claim 1, further comprising a row decoder to provide word lines for selecting rows of groups of memory cells, and a column decoder to activate bit lines connected to the groups of memory cells.

11. The storage device of claim 1, further comprising a row decoder to provide write word lines for selecting individual memory cells within each group.

12. The storage device of claim 1, wherein each memory cell is formed of a stack of layers, the stack having a first end and a second end, and wherein the memory cells of each group are arranged such that current flows from the first end to the second end in each of the memory cells of the first set.

13. The storage device of claim 1, wherein each group further comprises a second set of parallel connected memory cells, wherein each memory cell is formed of a stack of layers, the stack having a first end and a second end,

wherein the first set of memory cells are connected in parallel between a first bias signal and a common node such that the first end of each memory cell in the first set is connected to the first bias signal, and the second end of each memory cell in the first set is connected to the common node,

wherein the second set of memory cells are connected in parallel between a second bias signal and the common node such that the first end of each memory cell in the second set is connected to the second bias signal, and the second end of each memory cell in the second set is connected to the common node.

14. The storage device of claim 13, further comprising a bit line, wherein the common node is coupled to a gate of the transistor, and a source of the transistor is coupled to the bit line.

15. A system comprising:

a processor; and

a storage device coupled to the processor, the storage device comprising:

groups of memory cells, the memory cells comprising magnetoresistive elements,

bit lines each connected to corresponding plural groups of memory cells,

wherein each group of memory cells includes memory cells connected in parallel and coupled to a respective bit line.

16. The system of claim 15, wherein each group further includes a transistor connected to the memory cells of the group, the transistor to drive a respective bit line to a voltage based on a state of a selected one of the memory cells in the group.

17. The system of claim 16, wherein the transistor is a field effect transistor configured as a source follower amplifier.

18. The system of claim 16, wherein the transistor is a bipolar junction transistor configured as an emitter follower amplifier.

19. The system of claim 16, further comprising sensing devices coupled to respective bit lines to detect a state of a corresponding selected memory cell.

20. The system of claim 19, wherein the storage device further comprises:

a control circuit to perform a read operation by sensing a group of memory cells, and subsequently writing a selected memory cell to a predetermined state; and

a read circuit to detect whether the selected memory cell changes state in response to the write to the predetermined state, the read circuit to output an indicator of a state of the selected memory cell based on whether the state of the memory cell has changed.

21. The system of claim 15, wherein each group further comprises a second set of memory cells connected in parallel, wherein both of the first set of memory cells and the second set of memory cells are connected to a common node.

22. The system of claim 21, wherein each group comprises a transistor having a gate connected to a corresponding common node.

23. The system of claim 22, wherein each group of memory cells is coupled between a first bias voltage signal and a second bias voltage signal, wherein the group of memory cells is activated by setting one of the first and second bias voltage signals to a bias voltage, and setting the other one of the first and second bias voltage signals to a ground potential.

24. A method of reading data in a storage device, comprising:

selecting at least one of a plurality of groups of memory cells, the memory cells comprising magnetoresistive elements, wherein each group of memory cells includes a first set of memory cells connected in parallel and a second set of memory cells connected in parallel, the first and second sets of memory cells connected to a common node;

detecting a voltage at the common node of the selected group of memory cells; and

outputting an indicator of a data state in response to the detected voltage of the node.

25. The method of claim 24, wherein detecting the voltage comprises detecting a first voltage, the method further comprising:

writing a first memory cell to a first state;

measuring a second voltage at the common node; and

determining whether the first voltage differs from the second voltage,

wherein outputting the indicator is based on a difference between the first and second voltages.

26. The method of claim 24, further comprising:

driving a bit line to a voltage in response to the voltage of the common node.

27. The method of claim 26, further comprising a sense amplifier detecting a voltage level of the bit line.

28. The method of claim 27, further comprising:

during a read operation, the sense amplifier detecting a first voltage associated with the bit line corresponding to a state of a selected memory cell;

during the read operation, performing a write of the selected memory cell to a predetermined state; and

during the read operation, the sense amplifier detecting a second voltage associated with the bit line after writing the selected memory cell to the predetermined state.

29. The method of claim 28, further comprising:

comparing the first and second voltages;

outputting an indicator of a first logical state in response to determining that the first and second voltages are substantially the same; and

outputting an indicator of a second logical state in response to determining that the first and second voltages are different by greater than a predetermined amount.